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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,109	02/10/2004	Kun-Chih Wang	NAUP0559USA	2108

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,109	WANG ET AL.	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-5, 7 and 9-11 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Downey et al. (U.S. Pat. 6,717,270).

Regarding claims 1 and 9, Downey (figure 4) discloses an integrated circuit comprising:

an aluminum bonding pad 406 defined on a stress-buffering dielectric layer 441 (column 5, lines 39-42);

an intermediate metal layer 414 fabricated in a first inter-metal dielectric (IMD) layer 443 that is under the stress-buffering dielectric layer 441, and the intermediate metal layer being disposed directly under the aluminum bonding pad 406 and electrically connected to the aluminum bonding pad through a plurality of via plugs 465 integrated with the aluminum bonding pad;

at least one metal frame 412 fabricated in a second IMD layer 445 under the first IMD layer 443, the metal frame 412 being disposed directly under the intermediate metal layer 431; and

a portion of active circuit components of the integrated circuit (Active I/O circuitry) disposed directly under the metal frame 412 (column 5, lines 35-65).

As to the grounds of rejection under section 103(a), the method for damascened is an intermediate process step that does not affect the structure of the final device. See MPEP 2113 which discussed the handling of "product by process" claims and recommends the alternative (102/103) grounds of rejection. Therefore, the process limitation (damascened) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 4-5, Downey (figure 4) discloses wherein the stress-buffering dielectric layer 441 and a peripheral are of the bondable metal pad is covered by a passivation layer 403 wherein the passivation layer 403 is made of silicon nitride (column 5, lines 59-65).

Regarding claim 7, Downey (figure 4) discloses wherein the passivation layer has a window exposing a top surface area of the bondable metal pad.

Regarding claim 10, Downey (figure 4) discloses wherein the plural via plugs are made of aluminum (column 4, lines 46-49).

Regarding claim 11, Downey (figure 4) discloses wherein the metal frame 412 comprising copper (column 5, lines 55-57).

3. Claims 1, 4-5, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cook et al. (U.S. Pat. 6,022,791) in view of Sakihama et al. (U.S. Pat. 6,522,021).

Regarding claims 1 and 9, Cook (figure 6b) discloses an integrated circuit comprising:

an aluminum bonding pad (TV) defined on a stress-buffering dielectric layer (D6);

a damascened intermediate metal layer (M5) fabricated in a first inter-metal dielectric (IMD) layer (D5) that is under the stress-buffering dielectric layer (D6), and the damascened intermediate metal layer being disposed directly under the aluminum bonding pad (TV) and electrically connected to the aluminum bonding pad through a via plug (V5) integrated with the aluminum bonding pad;

at least one damascened metal frame (M4) fabricated in a second IMD layer (D4) under the first IMD layer, the damascened metal frame (M4) being disposed directly under the damascened intermediate metal layer (M5); and

a portion of active circuit components of the integrated circuit (S/D) disposed directly under the damascened metal frame. It is note that the process limitation (damascened) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Cook does not disclose more than one via plugs V5 connected to the bonding pad. However, Sakihama (in figure 12B) teaches a multi-layered metal wiring by using the underlying metal wiring connected to each of the via metal connecting regions (250a, 250b) (column 3, lines 45-50) to moderate the current concentration occurring in the metal wiring for connecting the bonding pad portion as to avoid an open failure caused by the electromigration (column3, lines 48-54). Accordingly, it would have been obvious to modify Cook's device by forming a plurality of via plugs connected to the bonding pad in order to avoid an open failure caused by the electromigration, as taught by Sakihama (column 3, lines 48-54).

Regarding claims 4-5, Cook (figure 6b) discloses wherein the stress-buffering dielectric layer (D6) and a peripheral are of the bondable metal pad is covered by a passivation layer wherein the passivation layer is made of nitride insulator (column 1, line 35).

Regarding claim 7, Cook (figure 6b) discloses wherein the passivation layer has a window exposing a top surface area of the bondable metal pad.

4. Claims 1, 4-5, 7-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pat. 6,731,007) in view of Sakihama et al. (U.S. Pat. 6,522,021).

Regarding claims 1 and 9-12, Saito (figure 1) discloses an integrated circuit comprising: an aluminum bonding pad BP (column 17, lines 6-11) defined on a stress-buffering dielectric layer 4d; an aluminum active circuit layer 13L, wherein the aluminum active circuit layer 13L and the aluminum bonding pad BP are defined on the stress-buffering dielectric layer 4d; a damascened intermediate copper layer $11L_2$ (column 18, lines1-3) fabricated in a first inter-metal dielectric 4C that is under the stress-buffering dielectric layer 4d, and the damascened intermediate copper layer $11L_2$ being disposed directly under the aluminum bonding pad BP and electrically connected to the aluminum bonding pad BP through an aluminum via plug $14C_2$ (column 17, lines 55-58) integrated with the aluminum bonding pad BP; at least one damascened copper frame $10C_2$ fabricated in a second IMD layer 10C under the first IMD layer 4C, the damascened copper frame $10C_2$ being disposed directly under the damascened intermediate copper layer $11L_2$; and a portion of active circuit components 3 of the integrated circuit disposed directly under the damascened metal frame $10C_2$. It is noted that the process limitation (damascened) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Saito does not disclose that more than one via plugs 14C connected to the aluminum-bonding pad BP.

However, Sakihama (figure 12B) teaches a multi-layered metal wiring by using the underlying metal wiring connected to each of the via metal connecting regions (250a, 250b) (column 3, lines 45-50) to moderate the current concentration occurring in

the metal wiring for connecting the bonding pad portion as to avoid an open failure caused by the electromigration (column3, lines 48-54). Accordingly, it would have been obvious to modify Saito's device by forming a plurality of via plugs connected to the bonding pad in order to avoid an open failure caused by the electromigration, as taught by Sakihama (column 3, lines 48-54).

Regarding claims 4-5, 7 and 15, Saito's figure 1 further discloses that the stress-buffering dielectric layer 4d, the aluminum active circuit layer 13L over the stress-buffering dielectric layer 4d, and a peripheral portions of the aluminum bonding pad BP are covered by a nitride passivation layer 15 (column 18, lines 16-20).

Regarding claim 8, Saito's figure 1 further discloses that the damascened intermediate metal layer $11L_2$ comprises copper conductor core (column 18, lines 6-9) and a diffusion barrier layer $11L_1$ disposed between the copper conductor core $11L_2$ and the first IMD layer 4C.

5. Claims 2-3 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pat. 6,731,007) and Sakihama et al. (U.S. Pat. 6,522,021) as applied to claims 1, 12 above, and further in view of Hashimoto et al. (U.S. 2003/0162354).

Neither Saito nor Sakihama discloses that the first and second IMD layers are less dense than the stress-buffering dielectric layer.

However, Hashimoto (figure 1) teaches the forming of the IMD layer 10 made of low-k dielectric (paragraph [0032]) and being less dense than the stress-buffering dielectric layer 11 made of high-k dielectric (silicon oxide) (paragraph [0032]). Accordingly, it would have been obvious to form the first and second IMD layers of Saito being less denser than the stress-buffering dielectric layer because as taught by Hashimoto, such less denser layer would have low relative permittivity in order to reduce the wiring capacitance (paragraph [0037]).

6. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pat. 6,731,007) and Sakihama et al. (U.S. Pat. 6,522,021) as applied to claims 4, 15 above, and further in view of Izumitani et al. (U.S. Pat. 6,727,590).

Neither Saito nor Sakihama discloses the passivation layer is made of polyimide.

However, Izumitani (figure 48) teaches the forming of the passivation layer 172/173 made of silicon nitride/polyimide (column 6, lines 25-31). Accordingly, it would have been obvious to form the passivation layer of Saito with silicon nitride/polyimide in order to provide a protective insulating film and the buffer coat insulating film, as taught by Izumitani (column 6, lines 25-31).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-

1704. The examiner can normally be reached on Monday to Thursday from 8:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
October 22, 2004.

PHAT X. CAO
PRIMARY EXAMINER